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as a mask; and

What Is Claimed Is:

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1 A method for fabricating a semiconductor device 2 having a dual damascene interconnecting line structure, 3 comprising the steps of: 4 providing a substrate having a dielectric layer thereon; 5 forming a first photoresist layer having a via contact hole 6 pattern on the dielectric layer; 7 forming a sacrificial layer on the first photoresist layer 8 and filling up the via contact hole pattern; 9 forming a second photoresist layer having an interconnect 10 trench pattern on the sacrificial layer, thereby 11 exposing sacrificial the layer beneath the 12 interconnect trench pattern; 13 transferring the interconnect trench pattern to the 14 sacrificial layer using the second photoresist layer

etching the first photoresist layer and the dielectric layer using the second photoresist layer as a mask, thereby transferring the interconnect trench pattern to the dielectric layer and forming an interconnect trench, and continuously etching the dielectric layer along the via contact hole pattern to form a via contact hole in the dielectric layer.

2. The method as claimed in claim 1, wherein the dielectric layer includes a material selected from the group consisting of SiO_2 , borosilicate glass (BSG), borophosphate silicate glass (BPSG), fluorosilicate glass (FSG), and tetra-ethyl-ortho-silicate (TEOS).

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- The method as claimed in claim 1, wherein the first
- 2 and second photoresists are chemically amplified silicon
- 3 photoresist.
- 1 4. The method as claimed in claim 1, wherein the first
- 2 and second photoresists are selected from different
- 3 photoresists.
- 1 5. The method as claimed in claim 1, wherein the
- 2 sacrificial layer is I-line photoresist.
- 1 6. The method as claimed in claim 1, wherein the depth
- of the interconnect trench is adjustable by altering etching
- 3 parameters, thereby changing the etching rate ratio of the first
- 4 or second photoresist and the etching rate of the sacrificial
- 5 layer.
- 1 7. The method as claimed in claim 1, wherein during
- 2 etching the sacrificial layer and the first photo resist, the
- 3 etching rates of the dielectric layer and the first photoresist
- 4 layer are equivalent.
- 8. A method for fabricating a semiconductor device
- 2 having a dual damascene interconnecting line structure,
- 3 comprising the steps of:
- 4 providing a substrate having a metal layer thereon;
- forming a dielectric layer on the metal layer;
- forming a first photoresist layer having a via contact hole
- 7 pattern on the dielectric layer;
- 8 forming a second photoresist layer on the first photoresist
- 9 layer and filling up the via contact hole pattern;

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- 10 forming a third photoresist layer having an interconnect 11 trench pattern on the second photoresist layer, 12 thereby exposing the second photoresist layer under 13 the interconnect trench pattern; 14 etching the second photoresist layer and transferring the 15 interconnect trench pattern into the photoresist layer using the third photoresist layer 16 17 as a mask; 18 etching the first photoresist layer and the dielectric 19 layer sequentially using the third photoresist layer 20 as a mask, thereby transferring the interconnect 21 trench pattern into the dielectric layer and forming 22 an interconnect trench, and continuously etching the 23 dielectric layer along the via contact hole pattern 24 to form a via contact hole in the dielectric layer; forming a conductive layer on the dielectric layer and 25 26 filling the via contact hole and the interconnect 27 trench; and 28 polishing the conductive layer until the dielectric layer 29 is exposed to achieve a damascene interconnecting 30 line structure with a via contact.
 - 1 9. The method as claimed in claim 8, wherein the 2 dielectric layer includes a material selected from the group 3 consisting of SiO₂, borosilicate glass (BSG), borophosphate 4 silicate glass (BPSG), fluorosilicate glass (FSG), and tetra-ethyl-ortho-silicate (TEOS). 5
 - 1 10. The method as claimed in claim 8, wherein the first 2 and the third photoresists are chemically amplified silicon 3 photoresist.

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- 1 11. The method as claimed in claim 8, wherein the first
- 2 and the third photoresists are selected from different
- 3 photoresists.
- 1 12. The method as claimed in claim 8, wherein the second
- 2 photoresist is I-line photoresist.
- 1 13. The method as claimed in claim 8, wherein the depth
- 2 of the interconnect trench is adjusted by altering etching
- 3 parameters, thereby changing the ratio of etching rates of the
- 4 first or third photoresist and the second photoresist.
- 1 14. The method as claimed in claim 8, wherein the etching
- 2 rate of the second photoresist is higher than the etching rate
- of the first/third photoresist, wherein the ratio of the etching
- 4 rates is about 5-15:1.
- 1 15. The method as claimed in claim 8, wherein during
- 2 etching the second photoresist and the first photoresist, the
- 3 etching rate of the dielectric layer and the etching rate of the
- 4 first photoresist are equal.
- 1 16. The method as claimed in claim 8, wherein the
- 2 conductive layer is metal.
- 1 17. The method as claimed in claim 8, wherein the
- 2 conductive layer is Au, Cu, Ag, Al, W, or alloys thereof.
- 1 18. The method as claimed in claim 9, wherein the
- 2 polishing step comprises chemical mechanical polishing (CMP).